SEMICONDUCTOR DEVICE WITH SUPERJUNCTION STRUCTURE

BACKGROUND OF THE INVENTION

[0001] A. Field of the Invention

[0002] The present invention relates to semiconductor devices having a superjunction structure, exhibiting a high breakdown voltage and a high current capability, and applicable to MOS-type field-effect transistors (hereinafter referred to as "MOSFET's"), insulated-gate bipolar transistors (hereinafter referred to as "IGBT's"), and bipolar transistors. Hereinafter, the semiconductor devices having a superjunction structure will be referred to sometimes as the "superjunction semiconductor devices."

[0003] B. Description of the Related Art

[0004] In the following descriptions, a superjunction semiconductor device is a semiconductor device that includes an alternating-conductivity-type layer including a column-shaped or layer-shaped p-type region and a column-shaped or layer-shaped n-type region adjoining each other repeatedly in parallel to the major surface of the semiconductor substrate. In other words, the alternating-conductivity-type layer is a drift layer that includes pn-junctions extending in perpendicular to the major surface of the semiconductor substrate. The drift layer that includes an alternating-conductivity-type layer makes a current flow in the ON-state of the device and sustains a bias voltage in the OFF-state of the device.

[0005] Generally, the semiconductor devices may be classified into a lateral semiconductor device and a vertical semiconductor device. In the lateral semiconductor device, the electrodes are formed on one major surface of a semiconductor substrate and a main current flows along the major surface. In the vertical semiconductor device, the electrodes thereof are distributed onto the major surfaces of a semiconductor substrate and a main current flows between the electrodes on the major surfaces.

[0006] In the vertical semiconductor device, the direction of a drift current flowing in the ON-state of the device is the same as the direction of a depletion layer expansion by a bias voltage in the OFF-state of the device. For example, the high resistivity n^- drift layer in the usual planar-type n-channel vertical MOSFET works as a region that makes a drift current flow vertically in the ON-state of the MOSFET and is depleted to sustain a bias voltage in the OFF-state of the MOSFET.

[0007] If the current path in the high resistivity n^- drift layer is short, the drift resistance will be low in the ON-state of the MOSFET. Therefore, the short current path is effective to lower the substantial ON-state resistance of the MOSFET. However, if the current path in the high resistivity n^- drift layer is short, the width, for which the depletion layer extending from the pn-junction between the p-type base region and the n^- drift layer expands in the OFF-state of the MOSFET, will be narrow, causing a low breakdown voltage. In order to obtain a semiconductor device with a high breakdown voltage, the n^- drift layer should be thick. A thick n^- drift layer causes high on-resistance and loss increase inevitably. In other words, there exists a tradeoff relationship between the on-resistance and the breakdown voltage. It is well known that the tradeoff relationship holds in the semiconductor devices such as IGBT's, bipolar transistors and diodes. The tradeoff relationship also holds commonly in the lateral semiconductor devices where the direction of the drift current flowing is different from the direction of the depletion layer expansion.

[0008] One way of solving the tradeoff relationship issue is to increase the impurity concentrations in the drift layer and to provide the drift layer with a superjunction structure that includes an alternating-conductivity-type layer including a n-type semiconductor region and a p-type semiconductor region arranged alternately. The superjunction semiconductor device forms the drift layer thereof of the alternating-conductivity-type layer described above to reduce the on-resistance and to deplete the drift layer quickly in the OFF-state further to make the depleted drift layer sustain a bias voltage. Therefore, the superjunction semiconductor device facilitates improving the tradeoff relationship described above.

[0009] The superjunction semiconductor device is different from the usual planar-type n-channel vertical MOSFET in that the drift layer in the superjunction semiconductor device is not a uniform layer of one conductivity-type but rather an alternating-conductivity-type layer including a column-shaped or layer-shaped n-type drift region and a column-shaped or layer-shaped p-type partition region adjoining each other repeatedly in parallel to the major surface of the semiconductor substrate to form a pn-junction therebetween and to extend the pn-junctions in perpendicular to the major surface of the semiconductor substrate. The impurity concentrations in the drift layer including n-type drift regions and p-type partition regions are set to be higher than the impurity concentration in the drift region in the usual vertical MOSFET exhibiting an almost equivalent breakdown voltage. The widths of the n-type drift region and p-type partition region are controlled to be narrow enough so that they are depleted by a lower bias voltage.

[0010] To provide a semiconductor device with a high breakdown voltage, it is necessary to form an edge-termination section that surrounds circularly the active section, in which the main current flows. If the edge termination section is not formed, the breakdown voltage will be low due to a high electric field in the edge area of the drift layer and it will be difficult to obtain a high breakdown voltage. Moreover, even if an initial high breakdown voltage is maintained by the provision of the edge termination section, it will be difficult for a semiconductor device that exhibits low robustness against induced charges to guarantee a long-term reliability for the breakdown voltage.

[0011] In a semiconductor device that exhibits low robustness against surface charges, the space charges induced onto the insulator film surface on the edge termination section affect the depletion layer expansion adversely and lower the breakdown voltage with the passage of time. In the following descriptions, the semiconductor device that exhibits high or excellent robustness against induced charges is a semiconductor device that facilitates suppressing the adverse effects of the charges, induced from the outside onto the insulator film surface on the edge termination section, on the depletion layer expansion in the edge termination section and keeping the initial breakdown voltage even after the passage of a predetermined operating time. In other words, the semiconductor device that exhibits high or excellent robustness against induced charges is a semiconductor device that exhibits a high reliability for breakdown voltage.

[0012] As a semiconductor device that improves the reliability for breakdown voltage thereof, a semiconductor